Cryogenic Wide-Band Ultra-Low-Noise IF Amplifiers Operating at Ultra-Low DC Power

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***Abstract*—This paper describes cryogenic broad-band amplifiers with very low power consumption and very low noise for the 4–8-GHz frequency range. At room temperature, the two-stage InP-based amplifier has a gain of 27 dB and a noise temperature of 31 K with a power consumption of 14.4 mW per stage, including bias circuitry. When cooled to 15 K, an input noise temperature of 1.4 K is obtained at 5.7 mW per stage. At 0.51 mW per stage, the input noise increases to 2.4 K. The noise measurements have been repeated at different laboratories using different methods and are found consistent.**

***Index Terms*—Cryogenic electronics, dc power, GaAs, InP high electron-mobility transistor (HEMT), low-noise amplifier (LNA), noise temperature.**

I. Introduction

InP-BASED high electron-mobility transistors (HEMTs) offer state-of-the-art low-noise performance and superior high-frequency performance [1]–[5]. The high mobility and carrier velocity in the InGaAs layer result in excellent performance at very low drain-to-source voltages. Furthermore, the HEMT technology does not suffer from the carrier freeze-out effect at low temperatures because the electrons reside in a quantum well of energy below the donor levels in the high bandgap material. This means that sufficient carrier densities for high gain microwave operation can be maintained even at temperatures as low as 15 K. Due to these characteristics, it is relevant to investigate the electrical behavior of different HEMTs at low dc power under cryogenic conditions. In this study, we have measured and compared the cryogenic noise performance of two different InP HEMT technologies, one lattice matched fabricated in-house and one pseudomorphic by TRW, Redondo Beach, CA (TRW4044–041), and a commercial pseudomorphic GaAs HEMT technology from Mitsubishi, Itami City, Japan (MGFC4419G). Amplifiers with ultra-low-noise and ultra-low dc power dissipation are of interest for deep space communication, where cooling and dc power budgets are restricted.

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II. HEMT Fabrication and Characteristics

TRW's InP HEMT epitaxial layer structures were grown by molecular beam epitaxy (MBE) on 3-in semi-insulating InP substrates. The single-side doped pseudomorphic 65% InGaAs channel HEMT structures were grown with channel electron density of $3.5 \cdot 10^{12}$ cm^{-2} and mobility of 11 000 cm^2/Vs at 300 K. The channel electron density and mobility measured at 77 K were $3.3 \cdot 10^{12}$ cm^{-2} and 42 000 cm^2/Vs, respectively. The low defect and trap density of the material is indicated since electron density at cryogenic temperature is high, similar to that at room temperature. This is an important factor for achieving good cryogenic device gain and noise performance. The wafers were processed using the baseline TRW InP HEMT production process with 0.1-μm gate length [6]. The baseline HEMT process includes device isolation by mesa etch, annealed ohmic contacts with a contact resistance of 0.1 Ωmm, electron-beam-lithography-defined 0.1-μm T-gates, PECVD silicon–nitride device passivation, 100-Ω/square thin-film resistors, 300-pF/mm^2 metal–insulator–metal (MIM) capacitors, and two levels of metal interconnect. In the InP HEMT backside process, wafers are thinned to 75 μm. Through-substrate vias are achieved using dry etching and provide connection from the backside ground plane to the frontside monolithic microwave integrated circuit (MMIC) elements. Backside metal is plated to 3-μm thickness.

The processing and device design have been tailored to maximize gain and minimize gate current, which are two important factors in optimizing devices for cryogenic noise performance. A key component in the HEMT fabrication is the control and repeatability of the gate process, which includes gate lithography, recess, and metallization. The 0.1-μm gate is defined by electron beam lithography in a bilayer of PMMA/P(MMA-MAA). The gate length is typically 0.1 μm with sigma of 0.01 μm. The gate recess is performed using a wet etchant. The etchant, combined with excellent adhesion of PMMA to the wafer, provides minimal lateral etching and, therefore, device gain and current are maximized since channel electron density is not depleted in the regions extrinsic to the gate. Furthermore, the impact of surface-related effects (traps) is minimized by limiting the lateral gate recess dimension. These factors contribute to high gain and good transport properties at cryogenic operation. The targeting of gate recess of the TRW InP HEMT devices to maximize gain while minimizing gate current is given in [7].

The device layouts consisted of a large variety of discrete coplanar InP HEMT devices with ground–signal–ground (GSG) configuration and 50-μm pad pitch. Dicing streets for die scribing were etched on the backside of the wafers. The room-temperature transconductance of the TRW InP HEMTs was $\sim$ 1200 mS/mm with cutoff frequencies greater than 220 GHz.

The Chalmers HEMT device used in the amplifier is based on a lattice-matched single-side doped structure on InP grown by MBE. Hall measurements were performed at 300 and 77 K. The low-field channel mobility was 8200 (27000) $cm^2V^{-1}s^{-1}$ and the sheet charge density was $1.6 \cdot 10^{12}$ $(1.9 \cdot 10^{12})$ cm^{-2} measured at 300 K (77 K).

The transistors were fabricated according to Chalmers standard InP HEMT process by a combination of optical and electron beam lithography techniques [8]. Mesa isolation was performed by wet chemical etching. The channel layer was selectively etched at the mesa sidewall. This decreases the gate leakage current since it prevents the gate electrode from contacting the channel at the mesa edge.

Ohmic contacts were formed by nickel, germanium, and gold (Ni/Ge/Au) with a source–drain spacing of 2 μm. Annealing was performed in a rapid thermal annealer (RTA). The resulting contact resistance was 0.2 Ωmm.

The 0.1-μm T-shaped gates were defined by electron beam lithography using a bilayer of PMMA/P(MMA-MAA). Special development patterns were used to control the developing time of the bottom layer. The gate recess was performed by wet etching. Titanium, platinum, and gold were evaporated to form the gate electrodes.

The definition of the transistor terminals was defined by a liftoff process using Ti/Au.

The devices were passivated with reactively sputtered silicon nitride. The deposition procedure is optimized in such a way that Schottky barriers remain unaffected and the introduction of interface states is negligible.

Plating was then used for air-bridge formation, connecting the source electrodes. In this step, additional metal was added to the pads to ensure good bonding ability. The wafer was lapped down to 80 μm and subsequently metallized by a liftoff procedure defining the dicing streets. The room-temperature transconductance of the Chalmers InP HEMTs was $\sim$ 550 mS/mm with cutoff frequencies greater than 100 GHz.

The Mitsubishi (MGFC4419G) GaAs devices are of pseudomorphic high electron-mobility transistor (pHEMT) type and have the same gatewidth (4×50 μm), but with 0.22-μm gate length. The average room-temperature transconductance was 440 mS/mm.

The three different HEMT chips are shown in Fig. 1. All devices have four gate fingers and a total gatewidth of 200 μm.

III. Modeling

Measurements of dc, S-parameters, and noise were carried out for each transistor, both at room temperature and 20-K ambient temperature. A small-signal model was extracted from this data [9]. The noise data was used to extract the noise model parameters [10]. In order to improve the accuracy of the noise measurements and to evaluate the model, a special pre-match circuit described in [11] was designed. All resistors, except R_{ds} (at temperature T_d), were set to ambient temperature. The extracted small-signal model together with T_d and the amplifier circuit were then used to calculate the expected noise and gain. The design of the amplifier and model development were done in parallel [11].

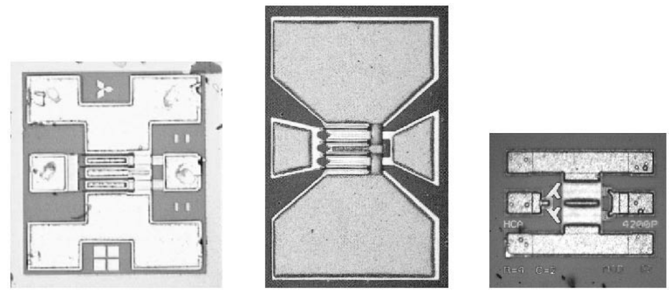

Fig. 1. HEMT chips used in the investigation. All devices have four gate fingers and a total gatewidth of 200 μm. The Chalmers device measures 300×200 μm^2. Chips are represented to scale.

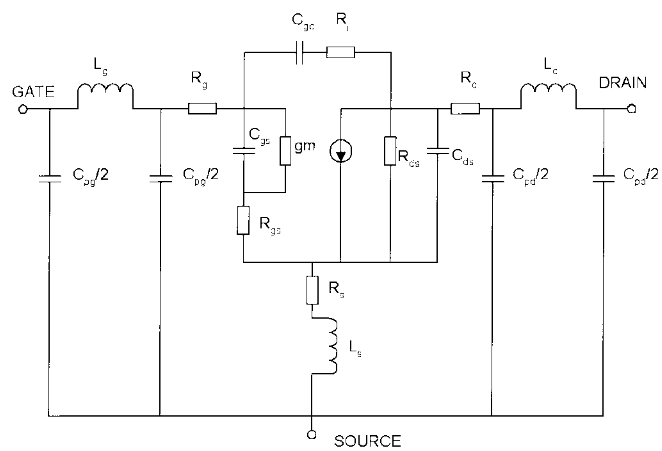

Fig. 2. Small-signal circuit used to model the transistors.

Fig. 2 shows the small-signal equivalent circuit used for all transistors. The parameter values for each transistor are shown in Table I. The pad parasitic values for the TRW transistor compared to Mitsubishi and Chalmers are lower due to the much smaller pads of the TRW transistor (Fig. 1). The differences in C_{gs}, C_{ds}, and C_{gd} are also notable. They can be made equal by tuning of V_{gs}.

IV. Amplifier Design

A two-stage 4–8-GHz single-ended amplifier with a specified gain of 26 dB was designed. The design was optimized for low noise at 15-K ambient temperature with constraints on the power consumption.

In order to facilitate the input match, an inductive feedback consisting of four 900-μm-long bond wires between the source of the transistor and ground was used. Stability problems were solved using resistive loading of the drains together with careful design of bias and inter-stage circuits. The amplifier was originally designed for the Mitsubishi MGFC4419G GaAs HEMT

TABLE I
EXTRACTED VALUES FOR THE SMALL-SIGNAL MODEL AT ROOM TEMPERATURE. UNITS ARE FEMTOFARAD, MILLISECOND, PICOHENRY, OHM, MILLIAMPERE, VOLT, AND KELVIN. THE T_d VALUES ARE AT 15 K

		MGFC4419G	TRW4044-041	Chalmers
Bias	V_{ds}	2.0	0.5	0.5
	I_{ds}	12.5	12.5	12.5
	V_{gs}	-0.25	+0.04	+0.03
Intrinsic	C_{gs}	125.3	103.9	120.9
	C_{ds}	58.5	57.1	65.6
	C_{gd}	49.3	41.3	40.0
	g_m	87.2	168.5	110.0
	R_{gs}	0.8	2.0	1.5
	R_j	0.3	10.7	0.3
	R_{ds}	200.0	54.1	102.0
Parasitics	C_{pg}, C_{pd}	6.3	4.6	6.0
	L_g	22.0	9.7	28.5
	L_s	1.6	0.5	1.7
	L_d	27.3	16.1	28.5
	R_g	1.0	1.0	1.0
	R_s	1.0	0.9	2.7
	R_d	1.5	2.0	3.2
Noise	T_d	1400	220	500

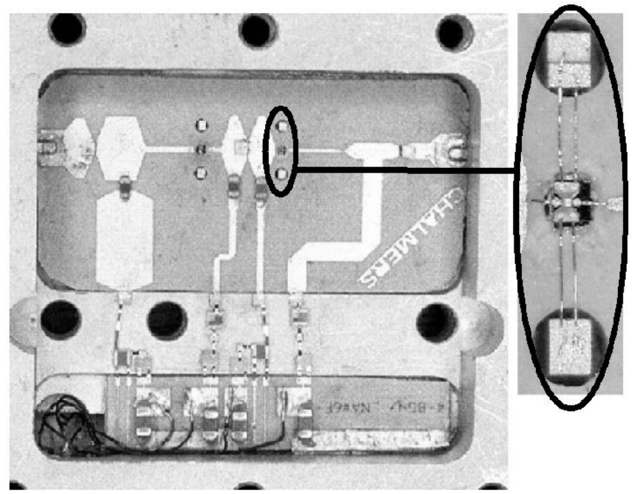

Fig. 3. Photograph of the mounted LNA and a magnified detail of the transistor mounting with inductive feedback bonding wires visible. The box measures 31 × 27 × 0.9 mm.

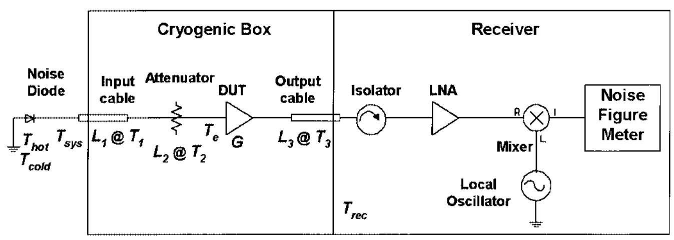

Fig. 4. Chalmers CAT system.

with 0.22×200 μm^2 gates, but the use of the InP transistors with the same gatewidth required only tuning of $V_{\rm gs}$ with the matching networks left unchanged. This is due to the similar input capacitances $C_{\rm gs}$ and optimum noise impedances of the devices. In addition, the inductive feedback reduced R_n making the design insensitive to input matching.

Several amplifiers were built in hybrid technology using microstrip transmission lines on a 30-mil-thick Rogers Duroid 6002 substrate. This substrate shows excellent temperature stability. Measurements of the dielectric constant using a 6-GHz resonator resulted $\varepsilon_r = 2.94$ (2.93) at 300 K (15 K). Fig. 3 shows a photograph of the amplifier and a close-up of one transistor with the inductive source feedback bonding wires.

V. EXPERIMENTAL

A. Measurement Setup

The cryogenic measurements were performed at 15 K at the Microwave Electronics Laboratory (MEL), Chalmers University of Technology, Göteborg, Sweden, using both a variable temperature load (VTL) and a cold attenuator (CAT) system (Fig. 4).

The Chalmers MEL VTL system consists of a coaxial 50-Ω termination with a heatable SMA-type 50-Ω load from Suhner and a temperature sensor mounted around the circular body. The load has a very weak thermal link to the cold plate, thus avoiding heating of the LNA in the "hot" state. $T_{\rm hot}$ and $T_{\rm cold}$ are approximately the same as in the CAT system. A short stainless-steel cable and a short copper cable with Teflon dielectric are connected between the load and the device-under-test (DUT). The noise contributions from the two cables are not compensated for. An HP8757D scalar network analyzer (SNA) is connected to the output via an isolator, low-noise amplifier (LNA), mixer, variable gain IF LNA, and precision variable attenuator. A synthesized sweeper (HP83752A) is used as a local oscillator (LO) for the mixer.

The noise source in the Chalmers MEL CAT system consists of a room-temperature 13.5-dB excess noise ratio (ENR) noise diode (HP 346B) in conjunction with a 23-dB attenuator cooled to 15 K. This gives a $T_{\rm cold} \approx 16.5$ K and a $T_{\rm hot} \approx 50$ K and a measured Y-factor of approximately 4.5 dB. Vacuum feedthroughs of SMA-type and 0.085-in stainless-steel inner and outer conductor cables with a Teflon dielectric (UT85-SS-SS) are used. An HP 8970B noise-figure meter (NFM) is connected to the output via an isolator, LNA, and mixer cascade. A synthesized sweeper (HP83620B) is used as an LO for the mixer.

B. Results

Fig. 5 shows the measured results of the LNA (#6H03) with InP transistors from TRW using the Chalmers CAT measurement system with corresponding biasing data in Table II. The Chalmers VTL system gave very similar results, typically within 0.3 K. The amplifier showed no signs of instability for 4–8 GHz with the input and output return loss typically better than 10 dB.

Fig. 6 shows the measured and simulated results of the same LNA (box and circuit) with three different sets of transistors (TRW InP, Chalmers InP, and Mitsubishi GaAs).

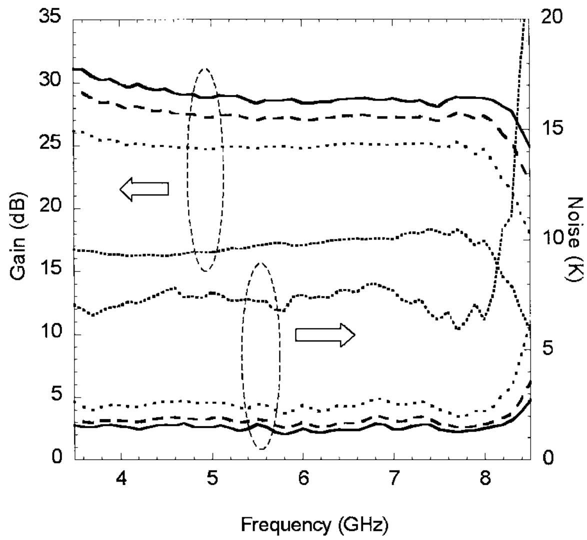

Fig. 5. Measured results at 14.8 K at different bias of amplifier #6H03 based on TRW 4044-041. From top to bottom: Gain at bias point 1 (BP1), BP2, BP3, BP4, noise at BP4, BP3, BP2, and finally, BP1. Corresponding bias points in Table II. The amplifier was measured at the MEL at Chalmers using a CAT system.

TABLE II
BIAS POINTS (BPs) AND DATA CORRESPONDING TO FIG. 5

	BP1	BP2	BP3	BP4
V_{d1}, V_{d2} [V]	1.15	0.5	0.3	0.1
I_{d1}, I_{d2} [mA]	5.0	3.0	1.7	0.5
P_{DC} [mW]	11.5	3.0	1.0	0.1
T_{avg} [K]	1.44	1.74	2.44	7.24

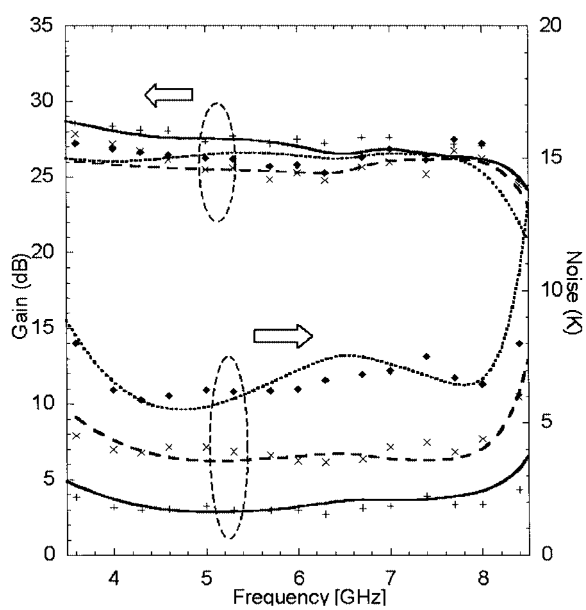

Fig. 6. Measured and simulated results of the LNA with different transistors. Simulated: TRW solid line, Chalmers dashed line, Mitsubishi dotted line. Measured: TRW +, Chalmers ×, and Mitsubishi ♦. The three upper curves show gain and the three lower curves shown the noise temperature.

The best results are achieved with the InP transistors from TRW and Chalmers. The TRW devices show the lowest noise performance with an average noise temperature of 1.4 K in the 4–8-GHz band with 11-mW dc power. When biased for lower dc power of 1.0 mW, the amplifier noise temperature was only 2.4 K. The Chalmers transistor required 3.7 mW and gave a noise temperature of 3.9 K. The commercial GaAs transistor from Mitsubishi, i.e., MGFC4419G, exhibited higher noise, i.e., 6.5 K, and required more dc power, i.e., 13.9 mW.

The LNAs are also working at room temperature, giving a low noise. The TRW transistor gives the best performance with an average noise temperature of 31 K and 27-dB gain in the 4–8-GHz band.

C. Measurement Uncertainty

Noise measurements at this level are quite difficult, and the obtained results have been validated by comparison of measurements at different research laboratories, i.e., Chalmers Radio and Space Science (RSS), Jet Propulsion Laboratory (JPL), California Institute of Technology (Caltech), and National Radio Astronomy Observatory (NRAO), and also by an uncertainty estimation.

The JPL CAT system was equipped with a 20-dB attenuator from Narda and in-house-made 7-mm vacuum feedthroughs and stainless-steel cables with air dielectric. The metal of the inner conductor is stainless steel and the inside of the cable is copper plated. Close to the DUT, a transition to a K-type connector was used followed by a short copper-plated stainless-steel 0.085-in cable. An HP 346B 15-dB ENR noise diode was used as noise source and an HP 8970B NFM was connected to the output via an HP8971 test set. A synthesized sweeper was used as an LO for the mixer. The worst case uncertainty of this measurement system has been estimated to ± 1.3 K [12].

In the Caltech VTL system, a coaxial 50-Ω load was used as the hot and cold noise source. $T_{\rm cold}$ was 4.2 K and the load was heated up to 20 K for $T_{\rm hot}$ using a resistive heater clamped around the load. The temperature of the load was measured using a Lakeshore DT-470 four-wire Si-diode, soldered to the body of the load. To avoid heating the cold plate, a weak thermal connection between the load and cold plate was used. A 5-in 0.141 SSI series-A cable (stainless-steel outer silver-coated copper-clad stainless-steel inner PTFE dielectric) was used between the load and DUT. The noise contribution from this cable was compensated for. The Y-factor was measured using an HP 8970A NFM.

The NRAO CAT system was also equipped with a 20-dB attenuator from Narda. In-house-made 0.120-in air-dielectric stainless-steel cables with gold-plated stainless-steel tube inner conductor and K-type vacuum feedthroughs with glass beads were used. An HP 346B 15-dB ENR noise diode was used as the noise source and an in-house-made NFM was connected to the output via an LNA and mixer cascade. An HP8350 sweeper was used as an LO for the mixer.

As can be seen from Table III, the agreement between the systems is very good, except for the result at the JPL, which differs from the other systems. The reason for this is not clear at the moment.

The difference in $T_{\rm ambient}$ is due to the individual properties of the cryo boxes. They are usually run at full capacity, resulting in different ambient temperatures. Noise measurements versus

TABLE III
AVERAGE NOISE TEMPERATURE IN THE 4–8-GHz BAND MEASURED AT DIFFERENT LABORATORIES. THE MEASUREMENTS WERE PERFORMED ON THE FIRST AMPLIFIER BUILT (#6G02). BIAS CONDITION IS $V_d = 1$ V AND $I_{d1} = I_{d2} = 5$ mA

Facility	T_{avg} [K]	$T_{ambient}$ [K]
JPL, 20dB attenuator	3.5	12.4
Caltech, VTL	2.3	4.2
Chalmers, Radio and Space Science, 23dB attenuator	2.2	10.2
Chalmers, Microwave Electronics Laboratory, VTL	2.1	16.8
NRAO, 20dB attenuator	2.1	15.2
Chalmers, Microwave Electronics Laboratory, 23dB attenuator	1.8	14.9

temperature show that T_e changes only approximately 0.1 K at ambient temperatures between 10–20 K.

The following uncertainty estimation is based on the Chalmers CAT system at the MEL (Fig. 4). The total equivalent noise temperature of the system ($T_{\rm sys}$) can be expressed as

$$T_{\rm sys} = (L_1 - 1)T_1 + (L_2 - 1)T_2L_1 + T_eL_1L_2 + \frac{(L_3 - 1)T_3L_1L_2}{G} + \frac{T_{\rm rec}L_1L_2L_3}{G} \quad (1)$$

where L_1–L_3 are losses associated with input cable, attenuator, and output cable at physical temperatures of T_1–T_3, respectively, G is the gain of the DUT, T_e is the equivalent noise temperature of the DUT, and $T_{\rm rec}$ is the equivalent noise temperature of the external receiver (often called second stage). Rearranging (1) gives (2), shown at the bottom of this page.

A sensitivity analysis for the determination of T_e has been performed and is summarized in Table IV. The main uncertainty contributors are the uncertainties associated with the input line and attenuator losses (L_1 and L_2), the ENR of the noise source, and the physical temperature of the attenuator (T_2). L_1 and L_2 are measured using an HP8510C vector network analyzer and the measurement uncertainty is estimated to ±0.1 dB. The measurement error of T_2 is typically ±0.5 K using a calibrated Lakeshore Cryogenics Thermometer together with a DT-470 diode sensor. Due to the uncertainty in the thermal contact between the diode sensor and the attenuator and possible temperature gradient between the outer conductor of the attenuator and the resistive elements inside, another 0.5 K is added to the T_2 tolerance. The input cable is heat sinked to 80 K close to the cryo box wall and to 15 K just before the attenuator. In the calculations cable temperatures of 80±20 K are assumed for both input and output sides. The ENR calibration table accuracy for the HP 346B 13.5-dB ENR noise diode is ±0.1 dB and is accounted for in the tolerances of $T_{\rm rec}$ and $T_{\rm sys}$. The accuracy of the Y-factor measurement using the HP8970B NFM is ±0.05 dB and is also

TABLE IV
MEASUREMENT UNCERTAINTY SOURCES IN THE 4–8-GHz FREQUENCY RANGE FOR THE EQUIVALENT INPUT NOISE TEMPERATURE T_e OF A DUT

Parameter	Nominal value	Tolerance	Resultant uncertainty in T_e, K
Input cable loss, L_1	0.5 dB	±0.1 dB	±0.41
Input cable physical temperature, T_1	80 K	±20 K	±0.03
Cryogenic attenuator loss, L_2	23 dB	±0.1 dB	±0.41
Cryogenic attenuator physical temperature, T_2	15 K	±1.0 K	±0.99
DUT gain, G	25 dB	±0.1 dB	±0.01
Output cable loss, L_3	0.5 dB	±0.1 dB	±0.01
Output cable physical temperature, T_3	80 K	±20 K	±0.02
Receiver noise, T_{rec}	80 K	±12 K	±0.04
System noise, T_{sys}	3900 K	±94 K	±0.42
RSS total errors			**±1.23**

included in the tolerances for $T_{\rm rec}$ and $T_{\rm sys}$. Error due to mismatch between the noise source and DUT are very difficult to estimate and has not been accounted for. Assuming the sources of the uncertainties are uncorrelated the resultant uncertainty can be summed in a root sum of squares fashion. A total uncertainty in T_e of ±1.2 K is obtained in this way (Table IV).

This uncertainty estimation is in good agreement with other published results. Fernandez [12] predicted a worst case uncertainty of ±1.3 K (RSS uncertainty of ±0.6 K) for the JPL system and Lopez–Fernandez *et al.* [13] have estimated ±1.4 K for a similar CAT system in Yebes, Spain. Risacher *et al.* [14] have investigated the CAT system of RSS with an RSS uncertainty of ±0.8 K.

VI. SUMMARY AND CONCLUSION

Recent work on cryogenically cooled HEMT-based LNAs has been presented. By thorough modeling and the availability of good devices, extraordinary low-noise performance at cryogenic temperatures has been achieved. A best minimum noise temperature of 1.4 K was achieved with an InP-based amplifier over the 4–8-GHz band with an associated gain of 27 dB. The power consumption was 5.7 mW per stage, including dc bias circuitry.

As expected, the InP-based amplifiers performed better than the GaAs-based amplifiers. This is mainly due to the superior carrier mobility and velocity of InP-based HEMTs, but in addition, the smaller gate length of the InP devices is beneficial for a high f_T at small current densities. The InP-based design then enables very low voltage and power biasing while preserving very low noise performance, especially in cryogenic operation.

The best results were achieved with the TRW devices that are especially designed for cryogenic operation. The use of a pseudomorphic MBE-grown epi-material with low defect and trap density results in a high electron mobility and density at cryogenic temperatures. The device design and fabrication process were also tailored for cryogenic low-noise operation.

$$T_e = \frac{T_{\rm sys} - (L_1 - 1)T_1 - (L_2 - 1)T_2L_1 - \dfrac{(L_3 - 1)T_3L_1L_2}{G} - \dfrac{T_{\rm rec}L_1L_2L_3}{G}}{L_1L_2} \quad (2)$$

Two important factors in this respect are maximized gain and minimized gate current. A low gate current operation is crucial for the lower frequency HEMT LNA applications (X-band) since gate current is a component contributing to shot noise. Decreased gate leakage current improves the overall cryogenic noise performance of the HEMTs, especially at lower frequencies.

To consolidate the results, measurements have been performed using different equipment at different laboratories with good agreement. More than 25 amplifiers have been manufactured during the study and the results are repeatable.

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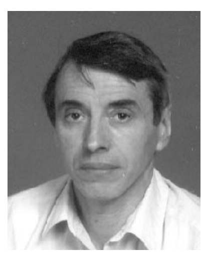

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Stacey Bui, photograph and biography not available at time of publication.

Emmanuil Choumas, photograph and biography not available at time of publication.

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